



PH20100S

N-channel TrenchMOS™ standard level FET

Rev. 02 — 17 August 2004

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low thermal resistance
- Low gate drive current
- SO8 equivalent area footprint
- Low on-state resistance.

1.3 Applications

- DC-to-DC converters
- Switched-mode power supplies

1.4 Quick reference data

- $V_{DS} \leq 100 \text{ V}$
- $I_D \leq 34.3 \text{ A}$
- $P_{tot} \leq 62.5 \text{ W}$
- $R_{DSon} \leq 23 \text{ m}\Omega$

2. Pinning information

Table 1: Discrete Pinning

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view</p> <p>SOT669 (LFPAK)</p>	<p>mbb076</p>
4	gate (g)		
mb	mounting base; connected to drain (d)		

3. Ordering information

Table 2: Ordering information

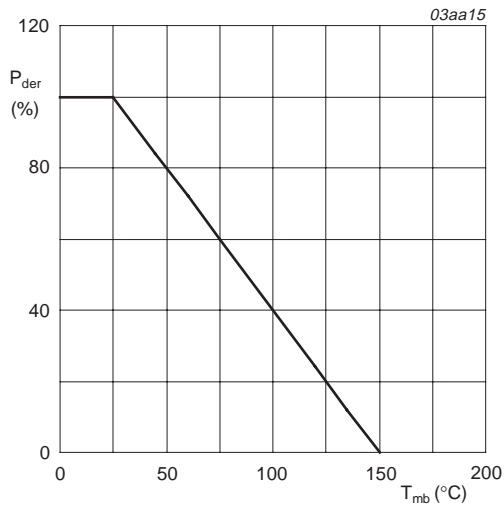
Type number	Package		Version
	Name	Description	
PH20100S	LFPAK	Plastic single-ended surface mounted package (Philips version LFPAK); 4 leads	SOT669

4. Limiting values

Table 3: Limiting values

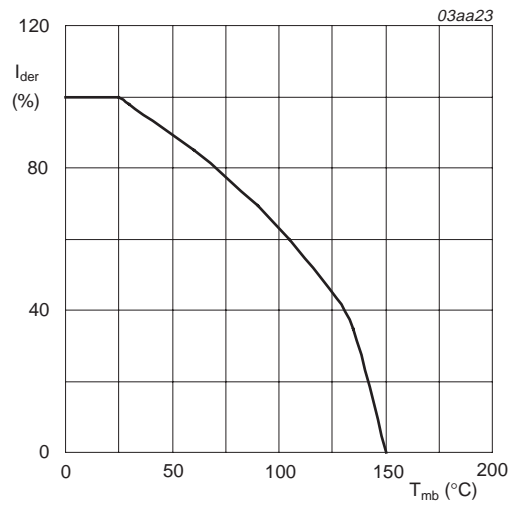
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	100	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2 and 3	-	34.3	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2	-	21.6	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	137	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	137	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 12\text{ A};$ $t_p = 0.3\text{ ms}; V_{DD} \leq 100\text{ V}; V_{GS} = 10\text{ V};$ starting at $T_j = 25\text{ °C}$	-	250	mJ



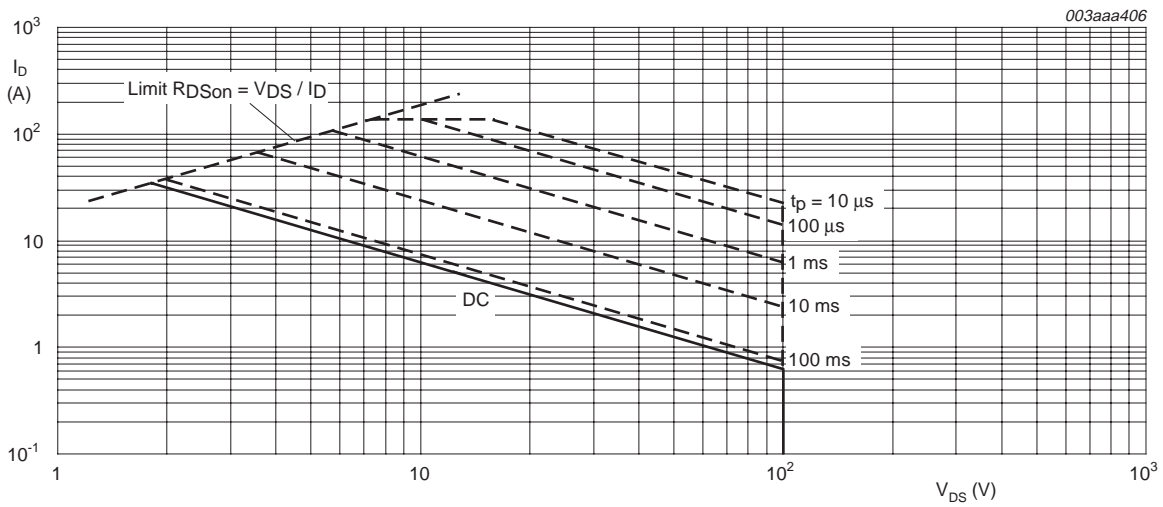
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 10 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance

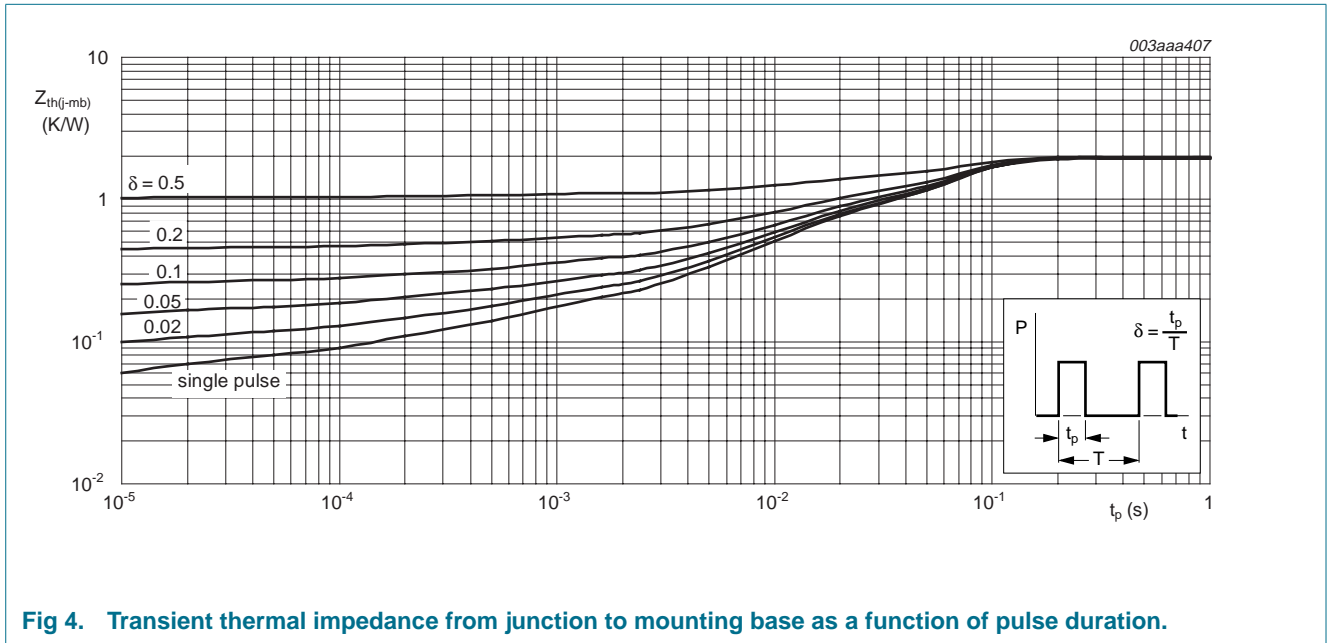


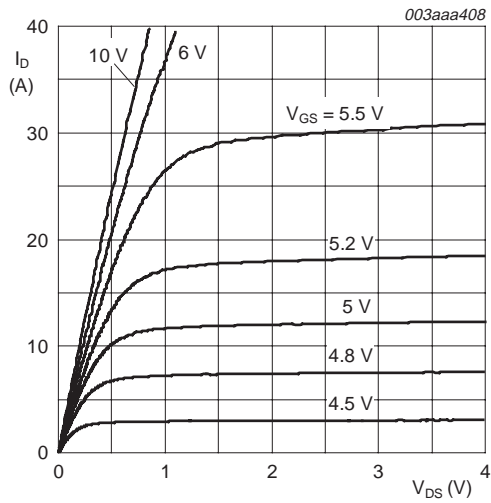
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

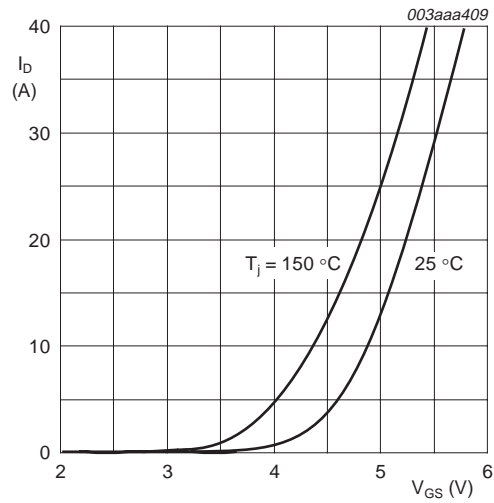
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 1\text{ mA}$; $V_{GS} = 0\text{ V}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 150\text{ °C}$	1.2	-	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 100\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.06	1	μA
		$T_j = 150\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	19	23	m Ω
		$T_j = 150\text{ °C}$	-	43	53	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 20\text{ A}$; $V_{DD} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; Figure 13	-	39	-	nC
Q_{gs}	gate-source charge		-	6.9	-	nC
Q_{gd}	gate-drain (Miller) charge		-	8.9	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; Figure 11	-	2264	-	pF
C_{oss}	output capacitance		-	290	-	pF
C_{rss}	reverse transfer capacitance		-	111	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 50\text{ V}$; $I_D = 10\text{ A}$; $V_{GS} = 10\text{ V}$; $R_G = 4.7\ \Omega$	-	23	-	ns
t_r	rise time		-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	47	-	ns
t_f	fall time		-	9.3	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$	-	110	-	ns



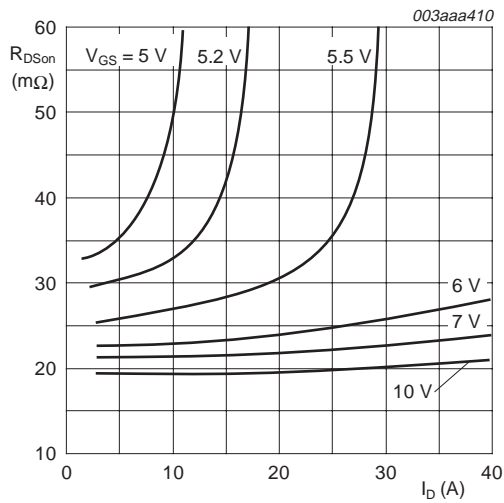
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



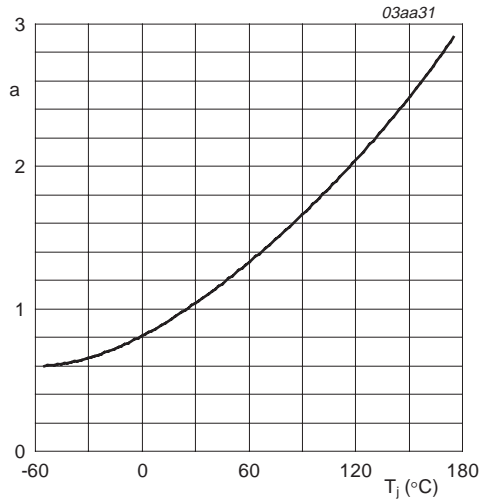
T_j = 25 °C and 150 °C; V_{DS} > I_D × R_{DSon}

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



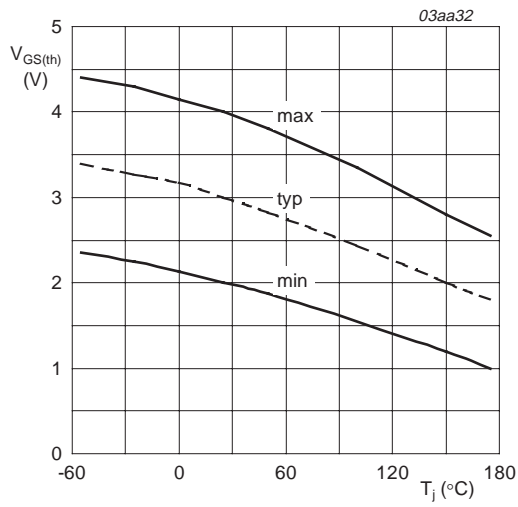
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



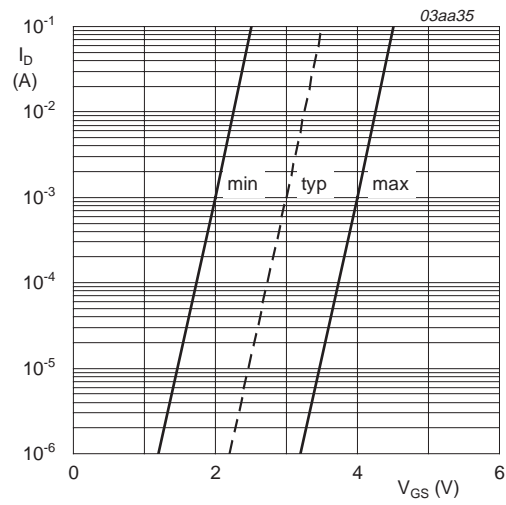
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



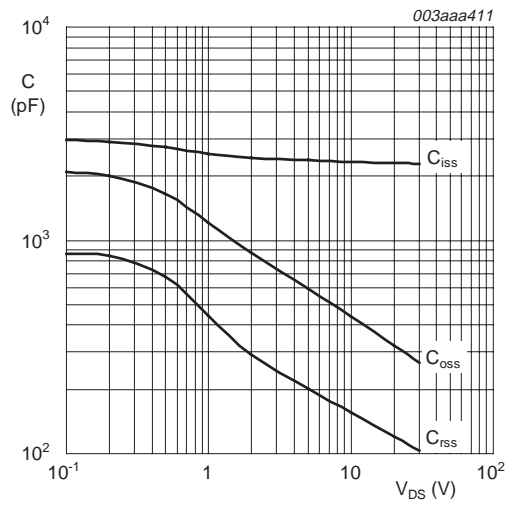
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



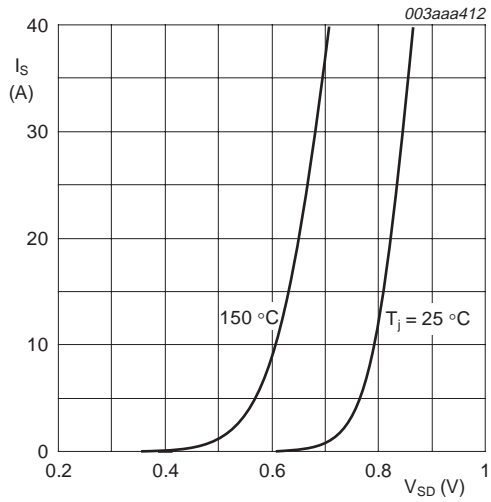
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



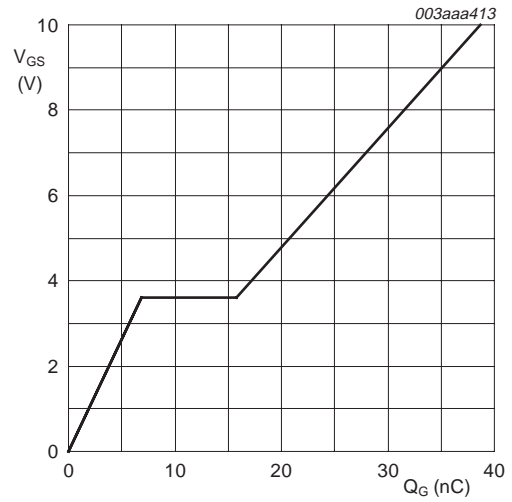
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



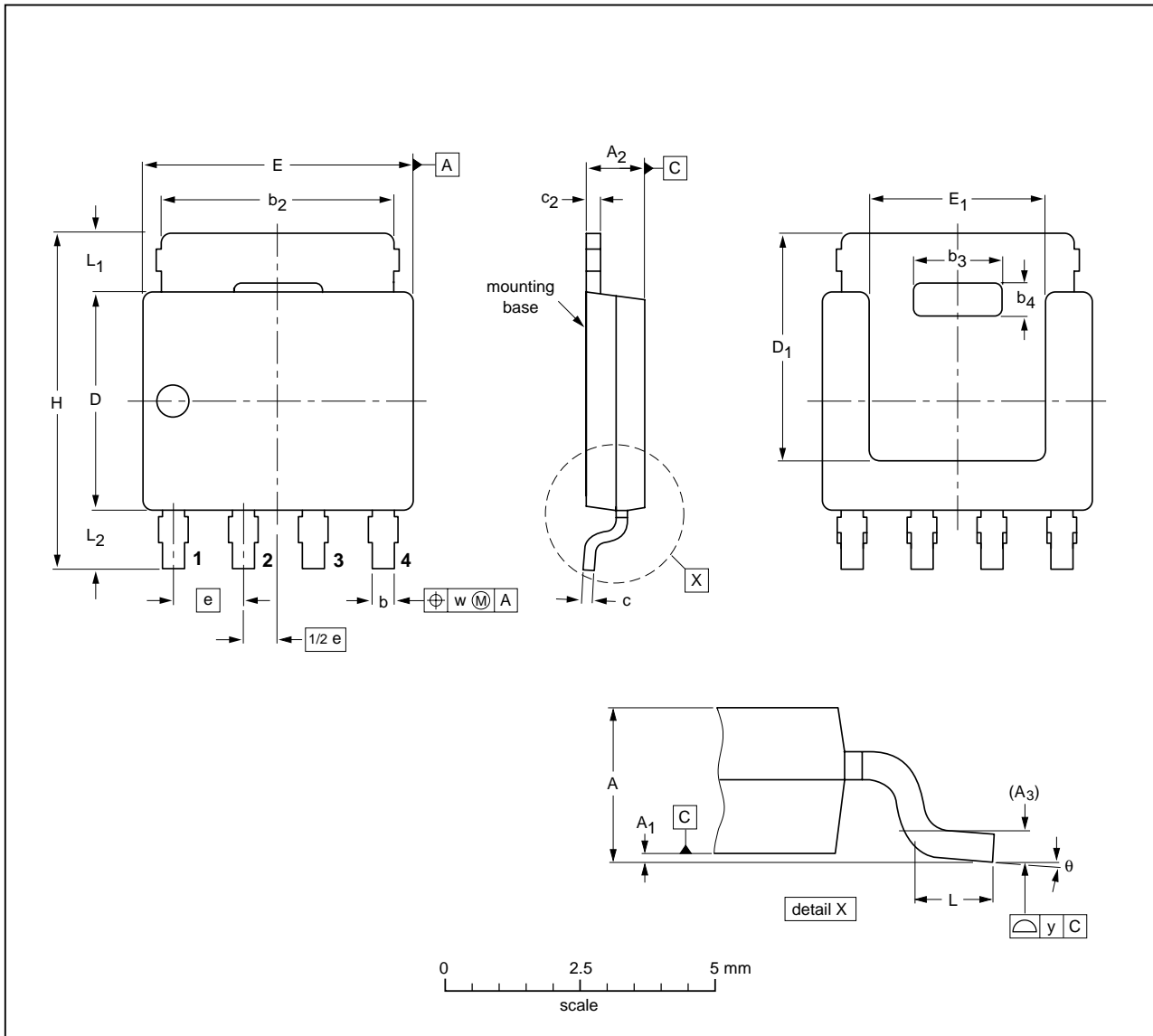
$I_D = 20\text{ A}$; $V_{DD} = 50\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic single-ended surface mounted package (Philips version LFPAK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾ max	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT669		MO-235			03-02-05 03-09-15

Fig 14. SOT669 (LFPAK).

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Document number	Supersedes
PH20100S_2	20040817	Product data sheet	-	9397 750 13698	PH20100S_1
Modifications:					<ul style="list-style-type: none"> • I_D max values updated in Section 1.4 "Quick reference data" and Section 4 "Limiting values" • R_{DSon} typ and max values updated in Section 1.4 "Quick reference data" and Section 6 "Characteristics" • Figure 3 and Figure 7 updated • Data sheet updated to latest standards.
PH20100S_1	20040305	Preliminary data sheet	-	9397 750 12815	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^[2] ^[3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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